

<b>INFORMATION DISCLOSURE STATEMENT</b>			Atty Docket: Serial No.: Applicant: Filing Date: Group:		02CT17653403 Not Yet Assigned LO IACONO Herewith		
<b>U.S. PATENT DOCUMENTS</b>							
Examiner Initials		Document Number	Date	Name	Class	Sub Class	Filing Date
TM	AA	4,534,010	8/6/85	Kobayashi et al.	364	748	
TM	AB	5,146,479	9/8/92	Okada et al.	377	41	
TM	AC	5,333,120	7/26/94	Gilber't	364	786	
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
<b>FOREIGN PATENT DOCUMENTS</b>							
		Document Number	Date	Country	Class	Sub Class	Translation
	AK						
	AL						
	AM						
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
TM	AN	Hashemian et al., A New Parallel Technique for Design of Decrement/Increment and Two's Complement Circuits, Proceedings of the Midwest Symposium on Circuits and Systems, Monterey, May 14-17, 1991, New York, US, Vol. 2 Symp. 34, May 14, 1991, Pages 887-890, XP000333546					
TM	AO	Sone et al., A 10-b 100-Msample/s Pipelined Subranging BiCMOS ADC, IEEE Journal of Solid-State Circuits, IEEE Inc. New York, US, Vol. 28, No. 12, December 1, 1993, Pages 1180-1186, XP000435890					
TM	AP	Stan et al., Synchronous Up/Down Counter with Clock Period Independent of Counter Size, Proceedings 13 <sup>th</sup> IEEE Symposium on Computer Arithmetic, CA, July 6-9, 1997, Pages 274-281, XP00788135					
TM	AQ	Parhami, Computer Arithmetic Algorithms and Hardware Designs, 2000, Oxford University Press, New York, XP002245799, Sections 5.2 and 5.5, Pages 78-80, 83-85					
<b>EXAMINER:</b> /Tan Mai/				<b>DATE CONSIDERED:</b> 10/09/2006			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.